## CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent.

1. A method of fabricating a MOSFET device having low-K dielectric oxide gate sidewall spacers formed by fluorine implantation, such that the implanted fluorine alters the properties of the gate sidewall spacers to develop a low parasitic capacitance MOSFET, comprising:

fabricating a MOSFET device structure;

forming a silicon nitride etch stop layer over the fabricated MOSFET device structure of the previous step;

depositing an oxide layer over the silicon nitride etch stop layer on the surfaces of the fabricated structure of the previous step to protect the substrate from a subsequent fluorine implant;

performing a fluorine implant through the silicon nitride etch stop layer and into the oxide gate sidewall spacers to form low-K fluorine doped oxide gate sidewall spacers.

2. The method of claim 1, wherein the step of performing a fluorine implant is performed with an implant dosage and implant energy to lower the dielectric constant of the MOSFET device from a value of substantially 4.0 to a value in the range of 3.3 to just below 4.0.

3. The method of claim 1, wherein the step of performing a fluorine implant is performed with an implant dosage and implant energy to achieve a dielectric constant for the MOSFET device of substantially 3.3.

4. The method of claim 1, further including stripping the oxide layer selective to the silicon nitride etch stop layer, and then oxidizing the silicon nitride layer to convert the silicon nitride etch stop to an oxide.

5. The method of claim 4, wherein the step of oxidizing the silicon nitride layer is performed with an ISSG oxidation process.

6. The method of claim 1, wherein the step of depositing includes depositing the oxide layer primarily on horizontal surfaces of the fabricated structure.

7. The method of claim 1, wherein the step of fabricating includes fabricating the MOSFET device on a silicon substrate by forming the shallow trench isolation STI, implanting the wells, forming the gate dielectric, and depositing and patterning the gate stack, implanting the source/drain extensions and forming the oxide gate sidewall spacers.

8. The method of claim 1, wherein the step of performing a fluorine implant comprises performing an angled, at an angle of 10 to 90 degrees relative to an upper horizontal surface of a wafer containing the MOSFET device, fluorine implant through the silicon nitride etch stop layer and into the oxide gate sidewall spacers to form the low-K fluorine doped oxide gate sidewall spacers.

9. The method of claim 1, wherein the step of performing a fluorine implant comprises performing an angled, at an angle of substantially 45 degrees relative to an upper horizontal surface of a wafer containing the MOSFET device, fluorine implant

through the silicon nitride etch stop layer and into the oxide gate sidewall spacers to form the low-K fluorine doped oxide gate sidewall spacers.

10. The method of claim 1, wherein the silicon nitride layer is deposited by chemical vapor deposition.

11. The method of claim 1, wherein the fluorine implant penetrates the oxide gate sidewall spacers and not the gate dielectric.

12. The method of claim 1, wherein the fluorine implant influences a junction/contact region of the MOSFET device to locally alter the gate dielectric characteristic, increasing the threshold voltage of the device.

13. The method of claim 1, wherein the step of performing a fluorine implant comprises performing an angled fluorine implant through the silicon nitride etch stop layer and into the oxide gate sidewall spacers to form the low-K fluorine doped oxide gate sidewall spacers.

14. The method of claim 13, wherein the fluorine implant penetrates the oxide gate sidewall spacers and not the gate dielectric.

15. The method of claim13, wherein the fluorine implant influences a junction/contact region of the MOSFET device to locally alter the gate dielectric characteristic, increasing the threshold voltage of the device.

16. A MOSFET device having fluorine doped low K dielectric oxide gate sidewall spacers, such that low-K properties of fluorine are used to develop a low parasitic capacitance MOSFET.

17. The MOSFET device of claim 16, having a dielectric constant value in the range of 3.3 to 4.0.

18. The MOSFET device of claim 16, having a dielectric constant value of substantially 3.3.

19. The MOSFET device of claim16, comprising a silicon substrate having shallow trench isolation STI, implanted wells, a gate dielectric, a deposited and patterned gate stack, implanted source/drain extensions and oxide gate sidewall spacers which are implanted with fluorine to form low-K fluorine doped oxide gate sidewall spacers.

20. The MOSFET device of claim 16, further including a silicon nitride oxide layer formed over the MOSFET device.